



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,284	11/21/2001	William Lo	MP0082	8191
26703 7590 07/22/2008 HARNESS, DICKEY & PIERCE P.L.C. 5445 CORPORATE DRIVE SUITE 200 TROY, MI 48098				
EXAMINER				
NGUYEN, TOAN D				
ART UNIT		PAPER NUMBER		
2616				
MAIL DATE		DELIVERY MODE		
07/22/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

09/991,284

Applicant(s)

LO, WILLIAM

Examiner

TOAN D. NGUYEN

Art Unit

2616

Period for Reply
-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) See Continuation Sheet is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 June 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

Continuation of Disposition of Claims: Claims pending in the application are 3-6, 13-19, 21-23, 28-34, 37-40, 46-52, 55-58, 65-72, 75-78, 85-91, 94-97, 104-111, 114-117, 124-130, 133-136, 143-150, 153-156 and 163-170.

Continuation of Disposition of Claims: Claims rejected are 3-6, 13-19, 21-23, 28-34, 37-40, 46-52, 55-58, 65-72, 75-78, 85-91, 94-97, 104-111, 114-117, 124-130, 133-136, 143-150, 153-156 and 163-170.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 3-6, 13-19, 21-23, 28-34, 37-40, 46-52, 55-58, 65-72, 75-78, 85-91, 94-97, 104-111, 114-117, 124-130, 133-136, 143-150, 153-156 and 163-170 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 68 and 69 are objected to because of the following informalities:

Claim 68, line 2, it is suggested to change "NIC" to --- GBIC ---. Similar problem exists in claim 69, line 4.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3-6, 13-19, 37-40 and 46-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Booth et al. (US 6,516,352) further in view of Huff (US 7,068,609).

For claims 3-6 and 13-19, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

a first device (figure 1, reference 10, page 2, paragraph [0006], lines 2-3) that communicates with a first media (figure 1, reference 20-1)(page 2, paragraph [0006], lines 5-10);

a second device (figure 1, reference 26-1, page 2, paragraph [0006], lines 9-10) that communicates with a second media (figure 1, reference 22-1)(page 2, paragraph [0006], lines 7-10); and

a Gigabit interface connector (GBIC) module (figure 1, reference 16-1, page 2, paragraph [0006], lines 5-8) that communicates with said first device (figure 1, reference 10) over said first media (figure 2, reference 20-1) and with said second device (figure 2, reference 26-1) over said second media (figure 2, reference 22-1), wherein said GBIC provides autonegotiation between said first and second devices (page 2, paragraph [0006], lines 5-10),

However, the applicant's admitted prior art (AAPA) does not expressly disclose: wherein said first device includes a first GBIC interface including a transmitter and a receiver, said GBIC module includes a second GBIC interface with a transmitter and a receiver, said GBIC module includes a first copper interface with a transmitter and a receiver, and said second device includes a second copper interface with a transmitter and a receiver;

wherein said transmitter of said first GBIC interface communicates with said receiver of said second GBIC interface and said receiver of said first GBIC interface

communicates with said transmitter of said second GBIC interface, said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface, and said transmitters of said first and second GBIC interfaces transmit a first configuration ordered set; and

wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst.

In an analogous art, Booth et al. disclose:

wherein said first device includes a first network interface card (NIC)(GBIC interface means) including a transmitter and a receiver (figures 8A-B, references 540A and 540B, col. 13, lines 28-45), said NIC (GBIC module means) includes a second NIC (GBIC interface means) with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15, lines 21-22), said NIC (GBIC module means) includes a first copper interface with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15, lines 21-22), and said second device (figure 5, reference 440) includes a second copper interface with a transmitter and a receiver (col. 15, lines 35-37);

wherein said transmitter of said first NIC (GBIC interface means) interface communicates with said receiver of said second NIC interface (GBIC interface means) and said receiver of said first NIC interface (GBIC interface means) communicates with

said transmitter of said second NIC interface (GBIC interface means) (figure 7, references 540A-B, col. 15, lines 28-51), said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface (figure 7, references 542A-B, col. 15, lines 28-56), and said transmitters of said first and second NIC interfaces (GBIC interfaces mean) transmit a first configuration ordered set (col. 16, lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5, line 2 as set forth in claim 3), wherein said first media includes 1000BASE-SX media (col. 4, line 67 as set forth in claim 4), wherein said first media includes 1000BASE-X media (col. 5, line 12 as set forth in claim 5), wherein said second media includes 1000BASE-T media (col. 5, line 23 as set forth in claim 6).

One skilled in the art would have recognized the wherein said first device includes a first NIC interface including a transmitter and a receiver, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Booth et al.'s network interface system and method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Booth et al. does not expressly disclose wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first

device that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst.

In an analogous art, Huff discloses wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst (col. 6, lines 14-17).

Huff further discloses wherein said first FLP burst contains at least one configuration parameter provided by said first configuration data (col. 6, lines 14-17 as set forth in claim 14); wherein said first copper interface and said second copper interface complete autonegotiation by exchanging additional data and establishing a link (col. 6, lines 14-17 as set forth in claim 15); wherein said transmitter of said second copper interface transmits second configuration data that is stored in said memory of said GBIC module (col. 6, lines 14-17 as set forth in claim 16); wherein said transmitter of said second GBIC interface generates a second configuration ordered set that contains at least one configuration parameter provided by said second configuration data (col. 6, lines 14-17 as set forth in claim 17); wherein said first and second GBIC interfaces establish a link (col. 6, lines 14-17 as set forth in claim 18); and wherein when said link between said first and second GBIC interfaces is lost, autonegotiation is initiated between said first and second GBIC interfaces, and wherein when said link between said first and second copper interfaces is lost, autonegotiation is initiated

between said first and second copper interfaces (col. 6, lines 14-17 as set forth in claim 19).

One skilled in the art would have recognized the wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

For claims 37-40 and 46-52, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

first means (figure 1, reference 10, paragraph [0006], lines 2-3) for communicating over with first media (figure 1, reference 20-1)(page 2, paragraph [0006], lines 5-10);

second means (figure 1, reference 26-1, page 2, paragraph [0006], lines 9-10) for communicating over with a second media (figure 2, reference 22-1)(page 2, paragraph [0006], lines 7-10); and

network interface means (figure 1, reference 16-1, page 2, paragraph [0006], lines 5-8) for communicating with said first means over said first media and with said

second means over said second media, and for providing autonegotiation between said first and second means (page 2, paragraph [0006], lines 5-10),

wherein said network interfacing means includes a Gigabit interface connector (GBIC) module for communicating with said first means and with said second means (figure 1, reference 16-1, page 2, paragraph [0006], lines 5-10).

However, the applicant's admitted prior art (AAPA) does not expressly disclose: wherein said first means includes a first network interfacing means including a transmitter and a receiver,

wherein said network interfacing means includes:

a second network interface with a transmitter and a receiver; and
a first copper interface with a transmitter and a receiver,

wherein said second means includes a second copper interface with a transmitter and a receiver,

wherein said transmitter of said first network *interface* communicates with said receiver of said second network interface and said receiver of said first network interface communicates with said transmitter of said second network interface,

wherein said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface,

wherein said transmitters of said first and second network interfaces transmit a first configuration ordered set, and

wherein after said receiver of said second network interface receives a second configuration ordered set from said transmitter of said first network interface and said network interfacing means stores in memory first configuration data of said first means that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst.

In an analogous art, Booth et al. disclose:

wherein said first means includes a first network interfacing means including a transmitter and a receiver (figures 8A-B, references 540A and 540B, col. 13, lines 28-45),

wherein said network interfacing means includes:

a second network interface with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15, lines 21-22); and

a first copper interface with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15, lines 21-22),

wherein said second means includes a second copper interface with a transmitter and a receiver (col. 15, lines 35-37),

wherein said transmitter of said first network interface communicates with said receiver of said second network interface and said receiver of said first network interface communicates with said transmitter of said second network interface (figure 7, references 540A-B, col. 15, lines 28-51),

wherein said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface

communicates with said transmitter of said second copper interface (figure 7, references 542A-B, col. 15 lines 28-56), and

wherein said transmitters of said first and second network interfaces transmit a first configuration ordered set (col. 16, lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5, line 2 as set forth in claim 37), wherein said first media includes 1000BASE-SX media (col. 4, line 67 as set forth in claim 38), wherein said first media includes 1000BASE-X media (col. 5, line 12 as set forth in claim 39), wherein said second media includes 1000BASE-T media (col. 5, line 23 as set forth in claim 40).

One skilled in the art would have recognized the wherein said first means includes a first network interfacing means including a transmitter and a receiver, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Booth et al.'s network interface system and method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Booth et al. does not expressly disclose wherein after said receiver of said second network interface receives a second configuration ordered set from said transmitter of said first network interface and said network interfacing means stores in memory first configuration data of said first means that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst.

In an analogous art, Huff disclose wherein after said receiver of said second network interface receives a second configuration ordered set from said transmitter of said first network interface and said network interfacing means stores in memory first configuration data of said first means that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst (col. 6, lines 14-17).

Huff further discloses wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst (col. 6, lines 14-17 as set forth in claim 47); wherein said first fast link pulse (FLP) burst generated by said first copper interface contains at least one configuration parameter provided by said first configuration data (as set forth in claim 48); wherein said first copper interface and said second copper interface complete 1000BASE-T autonegotiation by exchanging additional data and establishing a 1000BASE-T link (col. 6, lines 14-17 as set forth in claim 49); wherein said memory of said GBIC module stores second configuration data of said device (col. 6, lines 14-17 as set forth in claim 50); wherein said transmitter of said second GBIC interface generates a second configuration ordered set that contains at least one configuration parameter provided by said second configuration data (col. 6, lines 14-17 as set forth in claim 51); wherein said first GBIC interface and said second

GBIC interface complete 1000BASE-X autonegotiation and establish a 1000BASE-X link (col. 6, lines 14-17 as set forth in claim 52).

One skilled in the art would have recognized the wherein after said receiver of said second network interface receives a second configuration ordered set from said transmitter of said first network interface and said network interfacing means stores in memory first configuration data of said first means that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

6. Claims 21-23, 28-34, 55-58, 65-72, 75-78, 85-91, 94-97, 104-111, 114-117, 124-130, 133-136, 143-150, 153-156 and 163-170 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Heaton (US 5,922,052) and Booth et al. (US 6,516,352) further in view of Huff (US 7,068,609).

For claims 21-23 and 28-34, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

a switch (figure 1, reference 10, paragraph [0006], lines 2-3) that communicates with first media (figure 1, reference 20-1)(page 2, paragraph [0006], lines 5-8);

a device (figure 1, reference 26-1, page 2, paragraph [0006], lines 9-10) that communicates with a second media (figure 2, reference 22-1)(page 2, paragraph [0006], lines 7-10), and

a Gigabit interface connector (GBIC) module (figure 1, reference 16-1, page 2, paragraph [0006], lines 5-8) that communicates with said switch (figure 1, reference 10) over said first media (figure 1, reference 20-1) and with said device (figure 1, reference 26-1) over said second media (figure 2, reference 22-1), wherein said GBIC module allows autonegotiation between said switch and said device (page 2, paragraph [0006], lines 5-10).

However, the applicant's admitted prior art (AAPA) does not expressly disclose a second media that is a different type of media than said first media. In an analogous art, Heaton discloses a second media (figure 2, reference 160) that is a different type of media than said first media (figure 1, reference 150)(col. 4, lines 50-67).

One skilled in the art would have recognized the second media that is a different type of media than said first media, and would have applied Heaton's communication circuit 100 in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Heaton's fast Ethernet combination chaining of auto-negotiations for multiple physical layer capability in the AAPA with the motivation being to provide each of physical layer circuits 150 and 160 contains well known auto-negotiation features (col. 5, lines 15-16).

The applicant's admitted prior art (AAPA) in view of Heaton does not expressly disclose:

wherein said switch includes a first GBIC interface with a transmitter and a receiver, said GBIC module includes a second GBIC interface with a transmitter and a receiver and a first copper interface with a transmitter and a receiver, and said device includes a second copper interface with a transmitter and a receiver,

wherein said transmitter of said first GBIC interface communicates with said receiver of said second GBIC interface and said receiver of said first GBIC interface communicates with said transmitter of said second GBIC interface,

wherein said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface,

wherein said transmitters of said first and second GBIC interfaces transmit a first configuration ordered set, and

wherein said transmitter of said first copper interface does not transmit a fast link pulse (FLP) burst until said transmitter of said first GBIC interface transmits said first configuration ordered set.

In an analogous art, Booth et al. disclose:

wherein said switch includes a first NIC interface (GBIC interface means) with a transmitter and a receiver (figures 8A-B, references 540A and 540B, col. 13, lines 28-45), said NIC (GBIC module means) includes a second NIC interface (GBIC interface means) with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15, lines 21-22), and a first copper interface with a transmitter and a receiver (figure 8A-B,

references 610 and 612, col. 15, lines 21-22), and said device includes a second copper interface with a transmitter and a receiver (col. 15, lines 35-37),

wherein said transmitter of said first NIC interface (GBIC interface means) communicates with said receiver of said second NIC interface (GBIC interface means) and said receiver of said first NIC interface (GBIC interface means) communicates with said transmitter of said second NIC interface (GBIC interface means) (figure 7, references 540A-B, col. 15, lines 28-51), and

wherein said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface (figure 7, references 542A-B, col. 15, lines 28-56), wherein said transmitters of said first and second NIC interfaces (GBIC interfaces mean) transmit a first configuration ordered set (col. 16, lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5, line 2 as set forth in claim 21); wherein said first media includes 1000BASE-SX media (col. 4, line 67 as set forth in claim 22), wherein said first media includes 1000BASE-X media (col. 5, line 12 as set forth in claim 23).

One skilled in the art would have recognized the wherein said first device includes a first NIC interface including a transmitter and a receiver, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Booth et al.'s network interface

system and method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Heaton and Booth et al. does not expressly disclose wherein said transmitter of said first copper interface does not transmit a fast link pulse (FLP) burst until said transmitter of said first GBIC interface transmits said first configuration ordered set.

In an analogous art, Huff discloses wherein said transmitter of said first copper interface does not transmit a fast link pulse (FLP) burst until said transmitter of said first GBIC interface transmits said first configuration ordered set (col. 6, lines 14-17).

Huff further discloses wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst (col. 6, lines 14-17 as set forth in claim 29); wherein said first fast link pulse (FLP) burst generated by said first copper interface contains at least one configuration parameter provided by said first configuration data (as set forth in claim 30); wherein said first copper interface and said second copper interface complete 1000BASE-T autonegotiation by exchanging additional data and establishing a 1000BASE-T link (col. 6, lines 14-17 as set forth in claim 31); wherein said memory of said GBIC module stores second configuration data of said device (col. 6, lines 14-17 as set forth in claim 32); wherein said transmitter of said second GBIC interface generates a second configuration ordered set that contains

at least one configuration parameter provided by said second configuration data (col. 6, lines 14-17 as set forth in claim 33); wherein said first GBIC interface and said second GBIC interface complete 1000BASE-X autonegotiation and establish a 1000BASE-X link (col. 6, lines 14-17 as set forth in claim 34).

One skilled in the art would have recognized the wherein said transmitter of said first copper interface does not transmit a fast link pulse (FLP) burst until said transmitter of said first GBIC interface transmits said first configuration ordered set, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

For claims 55-58 and 65-72, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

coupling a first media (figure 1, reference 20-1) to a first device (figure 1, reference 10)(page 2, paragraph [0006]);

coupling a second media (figure 1, reference 22-1) to a second device (figure 1, reference 26-1)(page 2, paragraph [0006], lines 7-10); and

using a Gigabit interface connector (GBIC) module (figure 1, reference 16-1) to communicate with said first device (figure 1, reference 10) over said first media (figure 1, reference 20-1) and with said second device (figure 1, reference 26-1) over said second media (figure 1, reference 22-1), wherein said GBIC module allows

Art Unit: 2616

autonegotiation between said first and second devices (page 2, paragraph [0006], lines 5-10).

However, the applicant's admitted prior art (AAPA) does not expressly disclose wherein said second media is a different type of media than said first media. In an analogous art, Heaton discloses wherein said second media (figure 2, reference 160) is a different type of media than said first media (figure 2, reference 150)(col. 4, lines 50-67).

One skilled in the art would have recognized the wherein said second media is a different type of media than said first media, and would have applied Heaton's communication circuit 100 in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Heaton's fast Ethernet combination chaining of auto-negotiations for multiple physical layer capability in the AAPA with the motivation being to provide each of physical layer circuits 150 and 160 contains well known auto-negotiation features (col. 5, lines 15-16).

The applicant's admitted prior art (AAPA) in view of Heaton does not expressly disclose:

providing a first GBIC interface including a transmitter and a receiver in said first device;

providing a second GBIC interface with a transmitter and a receiver in said GBIC;

providing a first copper interface with a transmitter and a receiver in said GBIC;

providing a second copper interface with a transmitter and a receiver in said second device;

establishing communications between said transmitter of said first GBIC interface and said receiver of said second NIC interface and between said receiver of said first GBIC interface and said transmitter of said second GBIC interface;

establishing communications between said transmitter of said first copper interface and said receiver of said second copper interface and between said receiver of said first copper interface and said transmitter of said second copper interface;

transmitting a first configuration ordered set using said transmitters of said first and second GBIC interfaces; and

transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set.

In an analogous art, Booth et al. disclose:

providing a first NIC interface (GBIC interface means) including a transmitter and a receiver in said first device (figures 8A-B, references 540A and 540B, col. 13, lines 28-45);

providing a second NIC interface (GBIC interface means) with a transmitter and a receiver in said NIC (GBIC interface means)(figure 8A-B, references 610 and 612, col. 15, lines 21-22);

providing a first copper interface with a transmitter and a receiver in said NIC (GBIC interface means) (figure 8A-B, references 610 and 612, col. 15, lines 21-22);

providing a second copper interface with a transmitter and a receiver in said second device (col. 15, lines 35-37);

establishing communications between said transmitter of said first NIC interface and said receiver of said second NIC interface and between said receiver of said first NIC interface (GBIC interface means) and said transmitter of said second NIC interface (GBIC interface means)(figure 7, references 540A-B, col. 15, lines 28-51);

establishing communications between said transmitter of said first copper interface and said receiver of said second copper interface and between said receiver of said first copper interface and said transmitter of said second copper interface (figure 7, references 542A-B, col. 15, lines 28-56); and

transmitting a first configuration ordered set using said transmitters of said first and second NIC interfaces (GBIC interface means) (col. 16, lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5 line 2 as set forth in claim 55), wherein said first media includes 1000BASE-SX media (col. 4, line 67 as set forth in claim 56), wherein said first media includes 1000BASE-X media (col. 5, line 12 as set forth in claim 57), wherein said second media includes 1000BASE-T media (col. 5, line 23 as set forth in claim 58).

One skilled in the art would have recognized the providing a first GBIC interface including a transmitter and a receiver in said first device, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill

in the art at the time of the invention, to use Booth et al.'s network interface system and method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Heaton and Booth et al. does not expressly disclose transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set. In an analogous art, Huff discloses transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set (col. 6, lines 14-17).

Huff further discloses comprising inserting at least one configuration parameter provided by said first configuration data in said first FLP burst (col. 6, lines 14-17 as set forth in claim 66); completing autonegotiation by exchanging additional data and establishing a link between said first copper interface and said second copper interface (col. 6, lines 14-17 as set forth in claim 67); transmitting second configuration data that is stored in said memory of said NIC using said transmitter of said second copper interface (col. 6, lines 14-17 as set forth in claim 68); generating a second configuration

ordered set that contains at least one configuration parameter provided by said second configuration data using said transmitter of said second NIC interface (col. 6, lines 14-17 as set forth in claim 69); establishing a link between said first and second GBIC interfaces (col. 6, lines 14-17 as set forth in claim 70); initiating autonegotiation between said first and second GBIC interfaces when said link between said first and second GBIC interfaces is lost (col. 6, lines 14-17 as set forth in claim 71); initiating autonegotiation between said first and second copper interfaces when said link between said first and second copper interfaces is lost (col. 6, lines 14-17 as set forth in claim 72).

One skilled in the art would have recognized the transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

For claims 75-78 and 85-91, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

a first device (figure 1, reference 10) that communicates with a first media (figure 1, reference 20-1)(page 2, paragraph [0006], lines 5-8);

a second device (figure 1, reference 26-1) that communicates with a second media (figure 1, reference 22-1)(page 2, paragraph [0006], lines 7-10); and

a Gigabit interface connector module (GBIC)(figure 1, reference 16-1) that communicates with said first device (figure 1, reference 10) over said first media (figure 1, reference 20-1) and with said second device (figure 1, reference 26-1) over said second media (figure 1, reference 22-1), wherein said GBIC module provides autonegotiation between said first and second devices (page 2, paragraph [0006], lines 5-10).

However, the applicant's admitted prior art (AAPA) does not expressly disclose wherein said first media is a different media than said second media. In an analogous art, Heaton discloses wherein said first media (figure 2, reference 150) is a different media than said second media (figure 2, reference 160)(col. 4, lines 50-67).

One skilled in the art would have recognized the wherein said first media is a different media than said second media, and would have applied Heaton's communication circuit 100 in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Heaton's fast Ethernet combination chaining of auto-negotiations for multiple physical layer capability in the AAPA with the motivation being to provide each of physical layer circuits 150 and 160 contains well known auto-negotiation features (col. 5, lines 15-16).

The applicant's admitted prior art (AAPA) in view of Heaton does not expressly disclose:

wherein said first device includes a first GBIC interface including a transmitter and a receiver, said GBIC module includes a second GBIC interface with a transmitter and a receiver, said GBIC module includes a first copper interface with a transmitter and a receiver, and said second device includes a second copper interface with a transmitter and a receiver,

wherein said transmitter of said first GBIC interface communicates with said receiver of said second GBIC interface and said receiver of said first GBIC interface communicates with said transmitter of said second GBIC interface,

wherein said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface,

wherein said transmitters of said first and second GBIC interfaces transmit a first configuration ordered set, and

wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst.

In an analogous art, Booth et al. disclose:

wherein said first device includes a first NIC interface (GBIC interface means) including a transmitter and a receiver (figures 8A-B, references 540A and 540B, col. 13, lines 28-45), said NIC (GBIC module means) includes a second NIC interface (GBIC interface means) with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15 lines 21-22), said NIC (GBIC interface means) includes a first copper interface with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15, lines 21-22), and said second device (figure 5, reference 440) includes a second copper interface with a transmitter and a receiver (col. 15, lines 35-37),

wherein said transmitter of said first NIC interface (GBIC interface means) communicates with said receiver of said second NIC interface (GBIC interface means) and said receiver of said first NIC interface (GBIC interface means) communicates with said transmitter of said second NIC interface (GBIC interface means)(figure 7, references 540A-B, col. 15, lines 28-51),

wherein said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface (figure 7, references 542A-B, col. 15, lines 28-56), and

wherein said transmitters of said first and second NIC interfaces (GBIC interface means) transmit a first configuration ordered set (col. 16, lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5, line 2 as set forth in claim 75), wherein said first media includes 1000BASE-SX media (col. 4, line 67 as set forth in claim 76), wherein said first media

includes 1000BASE-X media (col. 5, line 12 as set forth in claim 77), wherein said second media includes 1000BASE-T media (col. 5, line 23 as set forth in claim 78).

One skilled in the art would have recognized the wherein said first device includes a first GBIC interface including a transmitter and a receiver, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Booth et al.'s network interface system and method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Heaton and Booth et al. does not expressly disclose wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst. In an analogous art, Huff discloses wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst (col. 6, lines 14-17).

Huff further discloses wherein said first FLP burst contains at least one configuration parameter provided by said first configuration data (col. 6, lines 14-17 as set forth in claim 86); wherein said first copper interface and said second copper

interface complete autonegotiation by exchanging additional data and establishing a link (col. 6, lines 14-17 as set forth in claim 87); wherein said transmitter of said second copper interface transmits second configuration data that is stored in said memory of said GBIC module (col. 6, lines 14-17 as set forth in claim 88); wherein said transmitter of said second GBIC interface generates a second configuration ordered set that contains at least one configuration parameter provided by said second configuration data (col. 6, lines 14-17 as set forth in claim 89); wherein said first and second GBIC interfaces establish a link (col. 6, lines 14-17 as set forth in claim 90); and wherein when said link between said first and second GBIC interfaces is lost, autonegotiation is initiated between said first and second GBIC interfaces, and wherein when said link between said first and second copper interfaces is lost, autonegotiation is initiated between said first and second copper interfaces (col. 6, lines 14-17 as set forth in claim 91).

One skilled in the art would have recognized the wherein after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the

motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

For claims 94-97 and 104-111, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

coupling a first media (figure 1, reference 20-1) to a first device (figure 1, reference 10)(page 2, paragraph [0006]);

coupling a second media (figure 1, reference 22-1) to a second device (figure 1, reference 26-1)(page 2, paragraph [0006], lines 7-10); and

using a Gigabit interface connector (GBIC) module (figure 1, reference 16-1) to communicate with said first device (figure 1, reference 10) over said first media (figure 1, reference 20-1) and with said second device (figure 1, reference 26-1) over said second media (figure 1, reference 22-1), wherein said GBIC module allows autonegotiation between said first and second devices (page 2, paragraph [0006], lines 5-10).

However, the applicant's admitted prior art (AAPA) does not expressly disclose wherein said second media is a different type of media than said first media. In an analogous art, Heaton discloses wherein said second media (figure 2, reference 160) is a different type of media than said first media (figure 2, reference 150)(col. 4, lines 50-67).

One skilled in the art would have recognized the wherein said second media is a different type of media than said first media, and would have applied Heaton's communication circuit 100 in the AAPA. Therefore, it would have been obvious to one of

ordinary skill in the art at the time of the invention, to use Heaton's fast Ethernet combination chaining of auto-negotiations for multiple physical layer capability in the AAPA with the motivation being to provide each of physical layer circuits 150 and 160 contains well known auto-negotiation features (col. 5, lines 15-16).

The applicant's admitted prior art (AAPA) in view of Heaton does not expressly disclose:

providing a first GBIC interface including a transmitter and a receiver in said first device;

providing a second GBIC interface with a transmitter and a receiver in said GBIC;

providing a first copper interface with a transmitter and a receiver in said GBIC;

providing a second copper interface with a transmitter and a receiver in said second device;

establishing communications between said transmitter of said first GBIC interface and said receiver of said second NIC interface and between said receiver of said first GBIC interface and said transmitter of said second GBIC interface;

establishing communications between said transmitter of said first copper interface and said receiver of said second copper interface and between said receiver of said first copper interface and said transmitter of said second copper interface;

transmitting a first configuration ordered set using said transmitters of said first and second GBIC interfaces; and

transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set.

In an analogous art, Booth et al. disclose:

providing a first NIC interface (GBIC interface means) including a transmitter and a receiver in said first device (figures 8A-B, references 540A and 540B, col. 13, lines 28-45);

providing a second NIC interface (GBIC interface means) with a transmitter and a receiver in said NIC (GBIC interface means)(figure 8A-B, references 610 and 612, col. 15, lines 21-22);

providing a first copper interface with a transmitter and a receiver in said NIC (GBIC interface means) (figure 8A-B, references 610 and 612, col. 15, lines 21-22);

providing a second copper interface with a transmitter and a receiver in said second device (col. 15, lines 35-37);

establishing communications between said transmitter of said first NIC interface and said receiver of said second NIC interface and between said receiver of said first NIC interface (GBIC interface means) and said transmitter of said second NIC interface (GBIC interface means)(figure 7, references 540A-B, col. 15, lines 28-51);

establishing communications between said transmitter of said first copper interface and said receiver of said second copper interface and between said receiver of

said first copper interface and said transmitter of said second copper interface (figure 7, references 542A-B, col. 15, lines 28-56); and

transmitting a first configuration ordered set using said transmitters of said first and second NIC interfaces (GBIC interface means) (col. 16, lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5 line 2 as set forth in claim 94), wherein said first media includes 1000BASE-SX media (col. 4, line 67 as set forth in claim 95), wherein said first media includes 1000BASE-X media (col. 5, line 12 as set forth in claim 96), wherein said second media includes 1000BASE-T media (col. 5, line 23 as set forth in claim 97).

One skilled in the art would have recognized the providing a first GBIC interface including a transmitter and a receiver in said first device, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Booth et al.'s network interface system and method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Heaton and Booth et al. does not expressly disclose transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set. In an analogous art, Huff discloses transmitting a first fast link pulse (FLP) burst using said

transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set (col. 6, lines 14-17).

Huff discloses further comprising inserting at least one configuration parameter provided by said first configuration data in said first FLP burst (col. 5, line 23 as set forth in claim 105); completing autonegotiation by exchanging additional data and establishing a link between said first copper interface and said second copper interface (col. 5, line 23 as set forth in claim 105); transmitting second configuration data that is stored in said memory of said GBIC using said transmitter of said second copper interface (col. 5, line 23 as set forth in claim 107); generating a second configuration ordered set that contains at least one configuration parameter provided by said second configuration data using said transmitter of said second GBIC interface (col. 5, line 23 as set forth in claim 108); establishing a link between said first and second GBIC interfaces (col. 5, line 23 as set forth in claim 109); initiating autonegotiation between said first and second GBIC interfaces when said link between said first and second GBIC interfaces is lost (col. 5, line 23 as set forth in claim 110); and initiating autonegotiation between said first and second copper interfaces when said link between said first and second copper interfaces is lost (col. 5, line 23 as set forth in claim 111).

One skilled in the art would have recognized the transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said

second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said first device that is contained in said second configuration ordered set, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

For claims 114-117 and 124-130, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

first means (figure 1, reference 10, paragraph [0006], lines 2-3) for communicating over with first media (figure 1, reference 20-1)(page 2, paragraph [0006], lines 5-8);

second means (figure 1, reference 26-1, page 2, paragraph [0006], lines 9-10) for communicating over with a second media (figure 2, reference 22-1)(page 2, paragraph [0006], lines 7-10); and

network interface means (figure 1, reference 16-1, page 2, paragraph [0006], lines 5-8) for communicating with said first means over said first media and with said second means over said second media, and for providing autonegotiation between said first and second means (page 2, paragraph [0006], lines 5-10), and

wherein said network interfacing means includes a Gigabit interface connector (GBIC) module (figure 1, reference 16-1, page 2, paragraph [0006], lines 5-10).

However, the applicant's admitted prior art (AAPA) does not expressly disclose wherein said first media is a different media than said second media. In an analogous art, Heaton discloses wherein said first media (figure 2, reference 150) is a different media than said second media (figure 2, reference 160)(col. 4, lines 50-67).

One skilled in the art would have recognized the wherein said first media is a different media than said second media, and would have applied Heaton's communication circuit 100 in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Heaton's fast Ethernet combination chaining of auto-negotiations for multiple physical layer capability in the AAPA with the motivation being to provide each of physical layer circuits 150 and 160 contains well known auto-negotiation features (col. 5, lines 15-16).

The applicant's admitted prior art (AAPA) in view of Heaton does not expressly disclose:

said first means includes a first interface including a transmitter and a receiver, said network interface means includes a second interface with a transmitter and a receiver, said network interface means includes a first copper interface with a transmitter and a receiver, and said second means includes a second copper interface with a transmitter and a receiver,

wherein said transmitter of said first interface communicates with said receiver of said second interface and said receiver of said first interface communicates with said transmitter of said second interface,

wherein said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface,

wherein said transmitters of said first and second interfaces transmit a first configuration ordered set, and

wherein after said receiver of said second interface receives a second configuration ordered set from said transmitter of said first interface and said network interface means stores in memory first configuration data of said first means that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst.

In an analogous art, Booth et al. disclose:

wherein said first means includes a first interfacing including a transmitter and a receiver (figures 8A-B, references 540A and 540B, col. 13, lines 28-45), said network interface means includes a second network interface with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15, lines 21-22), said network interface means includes a first copper interface with a transmitter and a receiver (figure 8A-B, references 610 and 612, col. 15, lines 21-22), and said second means includes a second copper interface with a transmitter and a receiver (col. 15, lines 35-37),

wherein said transmitter of said first network interface communicates with said receiver of said second network interface and said receiver of said first network interface communicates with said transmitter of said second network interface (figure 7, references 540A-B, col. 15, lines 28-51),

wherein said transmitter of said first copper interface communicates with said receiver of said second copper interface and said receiver of said first copper interface communicates with said transmitter of said second copper interface (figure 7, references 542A-B, col. 15, lines 28-56), and

wherein said transmitters of said first and second network interfaces transmit a first configuration ordered set (col. 16 lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5, line 2 as set forth in claim 114), wherein said first media includes 1000BASE-SX media (col. 4 line 67 as set forth in claim 115), wherein said first media includes 1000BASE-X media (col. 5 line 12 as set forth in claim 116), wherein said second media includes 1000BASE-T media (col. 5, line 23 as set forth in claim 117).

One skilled in the art would have recognized said first means includes a first interface including a transmitter and a receiver, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Booth et al.'s network interface system and method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Heaton and Booth et al. does not expressly disclose wherein after said receiver of said second interface receives a second configuration ordered set from said transmitter of said first interface and said network interface means stores in memory first configuration data of said first means that is contained in said second configuration ordered set, said

transmitter of said first copper interface transmits a first fast link pulse (FLP) burst. In an analogous art, Huff discloses wherein after said receiver of said second interface receives a second configuration ordered set from said transmitter of said first interface and said network interface means stores in memory first configuration data of said first means that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst (col. 6, lines 14-17).

Huff discloses wherein said first FLP burst contains at least one configuration parameter provided by said first configuration data (col. 5, line 23 as set forth in claim 125); wherein said first copper interface and said second copper interface complete autonegotiation by exchanging additional data and establishing a link (col. 5, line 23 as set forth in claim 126); wherein said transmitter of said second copper interface transmits second configuration data that is stored in said memory of said network interface means (col. 5, line 23 as set forth in claim 127); wherein said transmitter of said second interface generates a second configuration ordered set that contains at least one configuration parameter provided by said second configuration data (col. 5, line 23 as set forth in claim 128); wherein said first and second interfaces establish a link (col. 5, line 23 as set forth in claim 129); wherein when said link between said first and second interfaces is lost, autonegotiation is initiated between said first and second interfaces, and wherein when said link between said first and second (col. 5, line 23 as set forth in claim 130).

One skilled in the art would have recognized the wherein after said receiver of said second interface receives a second configuration ordered set from said transmitter

of said first interface and said network interface means stores in memory first configuration data of said first means that is contained in said second configuration ordered set, said transmitter of said first copper interface transmits a first fast link pulse (FLP) burst, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

For claims 133-136 and 143-150, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

coupling a first media (figure 1, reference 20-1) to a switch (figure 1, reference 10)(page 2, paragraph [0006]);

coupling a second media (figure 1, reference 22-1) to a device (figure 1, reference 26-1)(page 2, paragraph [0006], lines 7-10); and

using a Gigabit interface connector (GBIC) module (figure 1, reference 16-1) to communicate with said switch (figure 1, reference 10) over said first media (figure 1, reference 20-1) and with said device (figure 1, reference 26-1) over said second media (figure 1, reference 22-1), wherein said GBIC module allows autonegotiation between said switch and said device (page 2, paragraph [0006], lines 5-10).

However, the applicant's admitted prior art (AAPA) does not expressly disclose wherein said second media is a different type of media than said first media. In an analogous art, Heaton discloses wherein said second media (figure 2, reference 160) is

Art Unit: 2616

a different type of media than said first media (figure 2, reference 150)(col. 4, lines 50-67).

One skilled in the art would have recognized the wherein said second media is a different type of media than said first media, and would have applied Heaton's communication circuit 100 in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Heaton's fast Ethernet combination chaining of auto-negotiations for multiple physical layer capability in the AAPA with the motivation being to provide each of physical layer circuits 150 and 160 contains well known auto-negotiation features (col. 5, lines 15-16).

The applicant's admitted prior art (AAPA) in view of Heaton does not expressly disclose:

providing a first GBIC interface including a transmitter and a receiver in said switch;

providing a second GBIC interface with a transmitter and a receiver in said GBIC module;

providing a first copper interface with a transmitter and a receiver in said GBIC module;

providing a second copper interface with a transmitter and a receiver in said device;

establishing communications between said transmitter of said first GBIC interface and said receiver of said second GBIC interface and between said receiver of said first GBIC interface and said transmitter of said second GBIC interface;

establishing communications between said transmitter of said first copper interface and said receiver of said second copper interface and between said receiver of said first copper interface and said transmitter of said second copper interface; transmitting a first configuration ordered set using said transmitters of said first and second GBIC interfaces; and

transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set.

In an analogous art, Booth et al. disclose:

providing a first GBIC interface including a transmitter and a receiver in said switch (figures 8A-B, references 540A and 540B, col. 13, lines 28-45);

providing a second GBIC interface with a transmitter and a receiver in said GBIC (figure 8A-B, references 610 and 612, col. 15, lines 21-22);

providing a first copper interface with a transmitter and a receiver in said GBIC (figure 8A-B, references 610 and 612, col. 15, lines 21-22);

providing a second copper interface with a transmitter and a receiver in said device (col. 15 lines 35-37);

establishing communications between said transmitter of said first GBIC interface and said receiver of said second GBIC interface and between said receiver of said first

GBIC interface and said transmitter of said second NIC interface (figure 7, references 540A-B, col. 15, lines 28-51);

establishing communications between said transmitter of said first copper interface and said receiver of said second copper interface and between said receiver of said first copper interface and said transmitter of said second copper interface (figure 7, references 542A-B, col. 15, lines 28-56); and

transmitting a first configuration ordered set using said transmitters of said first and second GBIC interfaces (col. 16, lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5, line 2 as set forth in claim 133), wherein said first media includes 1000BASE-SX media (col. 4, line 67 as set forth in claim 134), wherein said first media includes 1000BASE-X media (col. 5 line12 as set forth in claim 135), wherein said second media includes 1000BASE-T media (col. 5 line 23 as set forth in claim 136).

One skilled in the art would have recognized the providing a first GBIC interface including a transmitter and a receiver in said switch, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Booth et al.'s network interface system and method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Heaton and Booth et al. does not expressly disclose transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second

GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set. In an analogous art, Huff discloses transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set (col. 6, lines 14-17).

Huff discloses further comprising inserting at least one configuration parameter provided by said first configuration data in said first FLP burst (col. 5, line 23 as set forth in claim 144); completing autonegotiation by exchanging additional data and establishing a link between said first copper interface and said second copper interface (col. 5, line 23 as set forth in claim 145); transmitting second configuration data that is stored in said memory of said GBIC module using said transmitter of said second copper interface (col. 5, line 23 as set forth in claim 146); generating a second configuration ordered set that contains at least one configuration parameter provided by said second configuration data using said transmitter of said second GBIC interface (col. 5, line 23 as set forth in claim 147); establishing a link between said first and second GBIC interfaces (col. 5, line 23 as set forth in claim 148); initiating autonegotiation between said first and second GBIC interfaces when said link between said first and second GBIC interfaces is lost (col. 5, line 23 as set forth in claim 149); initiating autonegotiation between said first and second copper interfaces when

said link between said first and second copper interfaces is lost (col. 5, line 23 as set forth in claim 150).

One skilled in the art would have recognized the transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

For claims 153-156 and 163-170, the applicant's admitted prior art (AAPA) discloses an autonegotiation circuit for Ethernet networks, comprising:

coupling a first media (figure 1, reference 20-1) to a switch (figure 1, reference 10)(page 2, paragraph [0006]);

coupling a second media (figure 1, reference 22-1) to a device (figure 1, reference 26-1)(page 2, paragraph [0006], lines 7-10); and

using a Gigabit interface connector (GBIC) module (figure 1, reference 16-1) to communicate with said switch (figure 1, reference 10) over said first media (figure 1, reference 20-1) and with said device (figure 1, reference 26-1) over said second media

(figure 1, reference 22-1), wherein said GBIC module allows autonegotiation between said switch and said device (page 2, paragraph [0006], lines 5-10).

However, the applicant's admitted prior art (AAPA) does not expressly disclose wherein said second media is a different type of media than said first media. In an analogous art, Heaton discloses wherein said second media (figure 2, reference 160) is a different type of media than said first media (figure 2, reference 150)(col. 4, lines 50-67).

One skilled in the art would have recognized the wherein said second media is a different type of media than said first media, and would have applied Heaton's communication circuit 100 in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Heaton's fast Ethernet combination chaining of auto-negotiations for multiple physical layer capability in the AAPA with the motivation being to provide each of physical layer circuits 150 and 160 contains well known auto-negotiation features (col. 5, lines 15-16).

The applicant's admitted prior art (AAPA) in view of Heaton does not expressly disclose:

providing a first GBIC interface including a transmitter and a receiver in said switch;

providing a second GBIC interface with a transmitter and a receiver in said GBIC module;

providing a first copper interface with a transmitter and a receiver in said GBIC module;

providing a second copper interface with a transmitter and a receiver in said device;

establishing communications between said transmitter of said first GBIC interface and said receiver of said second GBIC interface and between said receiver of said first GBIC interface and said transmitter of said second GBIC interface;

establishing communications between said transmitter of said first copper interface and said receiver of said second copper interface and between said receiver of said first copper interface and said transmitter of said second copper interface;

transmitting a first configuration ordered set using said transmitters of said first and second GBIC interfaces; and

transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set.

In an analogous art, Booth et al. disclose:

providing a first GBIC interface including a transmitter and a receiver in said switch (figures 8A-B, references 540A and 540B, col. 13, lines 28-45);

providing a second GBIC interface with a transmitter and a receiver in said GBIC (figure 8A-B, references 610 and 612, col. 15, lines 21-22);

providing a first copper interface with a transmitter and a receiver in said GBIC (figure 8A-B, references 610 and 612, col. 15, lines 21-22);

providing a second copper interface with a transmitter and a receiver in said device (col. 15 lines 35-37);

establishing communications between said transmitter of said first GBIC interface and said receiver of said second GBIC interface and between said receiver of said first GBIC interface and said transmitter of said second NIC interface (figure 7, references 540A-B, col. 15, lines 28-51);

establishing communications between said transmitter of said first copper interface and said receiver of said second copper interface and between said receiver of said first copper interface and said transmitter of said second copper interface (figure 7, references 542A-B, col. 15, lines 28-56); and

transmitting a first configuration ordered set using said transmitters of said first and second GBIC interfaces (col. 16, lines 35-37).

Booth et al. further disclose wherein said first media includes 1000BASE-LX media (col. 5, line 2 as set forth in claim 153), wherein said first media includes 1000BASE-SX media (col. 4, line 67 as set forth in claim 154), wherein said first media includes 1000BASE-X media (col. 5 line12 as set forth in claim 155), wherein said second media includes 1000BASE-T media (col. 5 line 23 as set forth in claim 156).

One skilled in the art would have recognized the providing a first GBIC interface including a transmitter and a receiver in said switch, and would have applied Booth et al.'s NIC in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Booth et al.'s network interface system and

method for dynamically switching between different physical layer devices in the AAPA with the motivation being to provide transceiver (col. 13, lines 28-45).

Furthermore, the applicant's admitted prior art (AAPA) in view of Heaton and Booth et al. does not expressly disclose transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set. In an analogous art, Huff discloses transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set (col. 6, lines 14-17).

Huff discloses comprising inserting at least one configuration parameter provided by said first configuration data in said first FLP burst configuration parameter provided by said second configuration data using said transmitter of said second GBIC interface (col. 5, line 23 as set forth in claim 164); completing autonegotiation by exchanging additional data and establishing a link between said first copper interface and said second copper interface (col. 5, line 23 as set forth in claim 165); transmitting second configuration data that is stored in said memory of said GBIC using said transmitter of said second copper interface (col. 5, line 23 as set forth in claim 166); generating a second configuration ordered set that contains at least one configuration parameter

provided by said second configuration data using said transmitter of said second GBIC interface (col. 5, line 23 as set forth in claim 167); establishing a link between said first and second GBIC interfaces (col. 5, line 23 as set forth in claim 168); initiating autonegotiation between said first and second GBIC interfaces when said link between said first and second GBIC interfaces is lost (col. 5, line 23 as set forth in claim 169); initiating autonegotiation between said first and second copper interfaces when said link between said first and second copper interfaces is lost (col. 5, line 23 as set forth in claim 170).

One skilled in the art would have recognized the transmitting a first fast link pulse (FLP) burst using said transmitter of said first copper interface after said receiver of said second GBIC interface receives a second configuration ordered set from said transmitter of said first GBIC interface and said GBIC module stores in memory first configuration data of said switch that is contained in said second configuration ordered set, and would have applied Huff's FLP in the AAPA. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Huff's method and apparatus for performing wire speed auto-negotiation in the AAPA with the motivation being performed auto-negotiation between two interfaces by using the FLP's (col. 6, lines 14-15).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOAN D. NGUYEN whose telephone number is (571)272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on 571-272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. D. N./
Examiner, Art Unit 2616

/FIRMIN BACKER/
Supervisory Patent Examiner, Art Unit 2616